In the claims.

1 – 4 (canceled)

5. (presently amended) A processor resetting apparatus comprising:

a fibre channel arbitrated loop (FC-AL) interface arranged to receive a frame containing an indicator of a reset command for a server including a processor associated with said resetting apparatus; and

a reset controller external to and distinct from the processor, responsive to said reset command, to issue a hardware reset interrupt command for resetting said processor.

6. (presently amended) A method for use with a system comprising first and second servers communicatively coupled over a fibre channel arbitrated loop (FC-AL) communications channel, each server comprising an FC-AL interfiace coupled to the FC-AL communications channel, and arranged to receive a frame containing an indicator of a reset command for a server including a processor associated with said resetting apparatus; and a reset controller, responsive to said reset command, to issue a reset interrupt command for resetting said processor; the method comprising the steps of:

at the first server, sending a frame over the FC-AL communications channel containing an indicator of a reset command addressed to the second server,

at the second server, receiving within a reset controller external to and distinct from the processor of the second server, the frame over the FC-AL communications channel containing the indicator of the reset command adddressed to the second server;

at the second server, in response to the receipt of the frame containing the indicator of the

reset command, issuing a hardware reset interrupt command from the reset controller to the processor of the second server;

whereby the processor of the second server is reset by means of the hardware reset interrupt command.